

Appl. No. 10/826,056  
Resp./Amdt. dated Aug. 10, 2005  
Reply to Office Action of 05/16/05

### Amendments to the Claims

This listing of claims will replace all prior versions, and listings, of claims in the application:

### Listing of Claims

Claim 1 (Currently amended): An imprinting apparatus comprising:

a semiconductor substrate polished in a [110] direction, the semiconductor substrate having a (110) horizontal planar surface and vertical sidewalls of a wet chemical etched trench, the trench vertical sidewalls are being aligned with (111) vertical lattice planes of the semiconductor substrate, ~~the semiconductor substrate comprising; and~~

a plurality of vertical structures disposed in the trench between the trench vertical sidewalls, a material of the vertical structures being different from a material of the semiconductor substrate,

~~wherein the trench vertical sidewalls and the plurality of vertical structures being~~ are spaced apart from each other and from the trench vertical sidewalls to form a mold that provides a pattern for imprinting.

Claim 2 (Original): The imprinting apparatus of Claim 1, wherein the semiconductor substrate is wet chemical etched along the (111) vertical lattice planes using an etching solution that etches the (111) vertical lattice plane much slower than a (110) horizontal lattice plane to form the trench.

Claim 3 (Original): The imprinting apparatus of Claim 1, wherein the semiconductor substrate is silicon, the etching solution being selected from potassium hydroxide, ethylene diamine pyrocatechol and tetramethylammonium hydroxide.

Claim 4 (Original): The imprinting apparatus of Claim 1, wherein the semiconductor substrate is a material selected from one of a Group IV element, Group III-V elements, and Group II-VI elements, the semiconductor substrate being wet chemical etched along the (111) vertical lattice planes.

Appl. No. 10/826,056  
Resp./Amdt. dated Aug. 10, 2005  
Reply to Office Action of 05/16/05

Claim 5 (Original): The imprinting apparatus of Claim 1, wherein the semiconductor substrate is wet chemical etched along the (111) vertical lattice planes such that the trench sidewalls have smooth surfaces relative to trench sidewalls that are dry chemical etched.

Claim 6 (Original): The imprinting apparatus of Claim 1, wherein the semiconductor substrate is wet chemical etched along the (111) vertical lattice planes such that the trench sidewalls have reduced crystal structure damage relative to trench sidewalls that are dry chemical etched.

Claim 7 (Original): The imprinting apparatus of Claim 1, wherein the semiconductor substrate is a silicon layer of a silicon-on-insulator wafer polished in the [110] direction.

Claim 8 (Currently amended): The imprinting apparatus of Claim 1, ~~wherein the plurality of vertical structures are nano-scale spaced using a deposited further comprising:~~

~~nano-scale thick layer layers of a first material alternating with a deposited nano-scale-thick layer of a second the vertical structure material in the trench, the first material being different from the semiconductor substrate material and the second vertical structure material, one of the first material layers being adjacent to the substrate the trench sidewall, the second material being adjacent the first material, the first material being selectively removed from between the trench sidewalls and vertically extending portions of the second material layers.~~

Claim 9 (Currently amended): The imprinting apparatus of Claim 8, wherein the semiconductor substrate is silicon, the first material being selected from silicon dioxide, silicon nitride and germanium, the ~~second vertical structure material being selected from silicon, silicon dioxide, silicon nitride and germanium, and wherein the first material is selectively removed from between the trench sidewalls and the vertically extending portions with an etchant that preferentially removes the first material instead of the silicon substrate and the second material.~~

Appl. No. 10/826,056  
Resp./Arndt. dated Aug. 10, 2005  
Reply to Office Action of 05/16/05

Claims 10 – 11 (Cancelled).

Claim 12 (Original): The imprinting apparatus of Claim 1, wherein the mold pattern has a vertical structure spacing in one or both of a nanometer range and a micrometer range.

Claim 13 (Currently amended): A nano-imprinting apparatus comprising:  
a semiconductor substrate having a horizontal (110) planar surface and a plurality of (111) vertical lattice planes intersecting the (110) planar surface;  
sidewalls of a trench etched in the semiconductor substrate along spaced apart (111) vertical lattice planes of the plurality using wet chemical etching, such that the trench sidewalls are (111) vertical planes; and  
a plurality of nano-scale spaced vertical structures disposed in the trench and spaced from the vertical trench sidewalls, a vertical structure of the plurality having opposing sides and an end, a side of the vertical structure facing one ~~or both~~ of a side of an adjacent vertical structure and a trench sidewall, the end having a horizontal surface coplanar with the (110) planar surface of the semiconductor substrate, a material of the plurality of vertical structures being different from a material the semiconductor substrate,

wherein the plurality of vertical structures between the trench sidewalls provides a nano-scale pattern for nano-imprinting.

Claim 14 (Original): The nano-imprinting apparatus of Claim 13, wherein the trench is wet chemical etched along the (111) vertical lattice planes using an etching solution that etches the (111) vertical lattice plane much slower than the (110) planar surface.

Claim 15 (Original): The nano-imprinting apparatus of Claim 14, wherein the semiconductor substrate is silicon, the etching solution being selected from potassium hydroxide, ethylene diamine pyrocatechol and tetramethylammonium hydroxide.

Appl. No. 10/826,056  
Resp./Amdt. dated Aug. 10, 2005  
Reply to Office Action of 05/16/05

Claim 16 (Original): The nano-imprinting apparatus of Claim 13, wherein the semiconductor substrate is a material selected from one of an element from Group IV, elements from Group III-V, and elements from Group II-VI.

Claim 17 (Original): The nano-imprinting apparatus of Claim 13, wherein the vertical sidewalls of the trench have one or both of smooth sidewalls and reduced crystal structure damage relative to trench sidewalls that are dry chemical etched.

Claim 18 (Original): The nano-imprinting apparatus of Claim 13, wherein the semiconductor substrate is a silicon layer of a silicon-on-insulator wafer polished in a [110] direction.

Claim 19 (Original): The nano-imprinting apparatus of Claim 13, wherein the vertical structures comprise a material selected from silicon, silicon dioxide, silicon nitride and germanium deposited in the trench by a chemical vapor deposition.

Claim 20 (Currently amended): The nano-imprinting apparatus of Claim 13, ~~wherein the vertical structures are nano-scale spaced using further comprising:~~

deposited nano-scale thick layers of a first material alternating with deposited nano-scale thick layers of ~~a second~~ the vertical structure material in the trench, the first material being different from the material of the semiconductor substrate and the ~~second vertical structure material~~, one of the first material layers being adjacent to the ~~trench sidewall semiconductor substrate, the second material being adjacent the first material, the first material being selectively removed from between the trench sidewalls and vertically extending portions of the second material layers in the trench.~~

Claim 21 (Currently amended): The nano-imprinting apparatus of Claim 20, wherein the semiconductor substrate is silicon, the first material being selected from silicon dioxide, silicon nitride and germanium, the ~~second vertical structure material~~ being selected from ~~silicon~~, silicon dioxide, silicon nitride and germanium.

Claims 22 – 23 (Cancelled).

Appl. No. 10/826,056  
Resp./Amdt. dated Aug. 10, 2005  
Reply to Office Action of 05/16/05

**Claim 24 (Original):** The nano-imprinting apparatus of Claim 13, wherein the nano-scale pattern has one or both of a vertical structure spacing that ranges from about 5 nm to about 100  $\mu\text{m}$  and a vertical structure pitch that ranges from about 10 nm to about 200  $\mu\text{m}$ .

**Claims 25 - 42 (Cancelled).**

**Claim 43 (New):** The imprinting apparatus of Claim 8, wherein the first material layers have a thickness that defines spaces between the vertical structures of the plurality and further defines spaces between each trench sidewall and a vertical structure of the plurality that is adjacent to the trench sidewall.

**Claim 44 (New):** The imprinting apparatus of Claim 8, wherein the vertical structure material layer has vertically extending portions that are the vertical structures of the plurality.

**Claim 45 (New):** The imprinting apparatus of Claim 8, wherein the first material layers and the vertical structure material layer define an internal depth of the imprinting apparatus.

**Claim 46 (New):** The imprinting apparatus of Claim 13, further comprising:

layers of a first material alternating with layers of the vertical structure material in the trench, the first material layers and the vertical structure material layers in the trench defining an internal depth of the imprinting apparatus.

**Claim 47 (New):** The imprinting apparatus of Claim 46, wherein the layers of vertical structure material have vertically extending portions that are the plurality of vertical structures.

**Claim 48 (New):** The imprinting apparatus of Claim 46, wherein the first material layers have a thickness that defines spaces between the vertical structures of the plurality and defines spaces between each trench sidewall and a vertical structure of the plurality adjacent to the trench sidewall.

Appl. No. 10/826,056  
Resp./Amtd. dated Aug. 10, 2005  
Reply to Office Action of 05/16/05

**Claim 49 (New):** The imprinting apparatus of Claim 20, wherein the nano-scale thickness of the first material layers define spaces between the vertical structures of the plurality and define spaces between each trench sidewall and a vertical structure of the plurality adjacent to the trench sidewall.

**Claim 50 (New):** An imprinting apparatus comprising:  
a semiconductor substrate polished in a [110] direction, the semiconductor substrate having a trench with vertical sidewalls, the sidewalls being aligned with (111) vertical lattice planes of the semiconductor substrate; and  
a plurality of vertical structures disposed in the trench between the sidewalls, a material of the vertical structures being distinct from a material of the semiconductor substrate,  
wherein the vertical structures are spaced apart from each other and from the sidewalls of the trench to form a mold that provides a pattern for imprinting.

**Claim 51 (New):** The imprinting apparatus of Claim 50, further comprising:  
a first material disposed in the trench that is different from the vertical structure material and the substrate material, the first material being between some of the vertical structures of the plurality to define spaces between the vertical structures, the first material further being between each sidewall of the trench and an adjacent vertical structure of the plurality to define spaces between the sidewalls and the adjacent vertical structures, the first material defining an internal depth of the imprinting apparatus.

**Claim 52 (New):** The imprinting apparatus of Claim 50, further comprising:  
alternating layers of a first material and the vertical structure material in the trench, the first material being different from the vertical structure material and the substrate material, one of the first material layers being adjacent to the substrate, the alternating layers defining an internal depth of the imprinting apparatus.

Appl. No. 10/826,056  
Resp./Amdt. dated Aug. 10, 2005  
Reply to Office Action of 05/16/05

**Claim 53 (New):** The imprinting apparatus of Claim 52, wherein the layers of the vertical structure material have vertical portions corresponding to the vertical structures of the plurality, a thickness of the first material layers defining spaces between the vertical structures of the plurality and further defining spaces between each sidewall and a vertical structure of the plurality that is adjacent to the sidewall.

**Claim 54 (New):** An imprinting apparatus comprising:  
a semiconductor substrate polished in a [110] direction, the semiconductor substrate having a trench with vertical sidewalls, the sidewalls being aligned with (111) vertical lattice planes of the semiconductor substrate;  
a plurality of vertical structures disposed in the trench between the sidewalls, and  
alternating layers of a first material and a second material in the trench, the second material layers having portions that extend vertically, the vertically extending portions being the plurality of vertical structures,  
wherein the vertical structures are spaced apart from each other and from the sidewalls of the trench to form a mold that provides a pattern for imprinting.

**Claim 55 (New):** The imprinting apparatus of Claim 54, wherein one of the first materials is adjacent to the semiconductor substrate in the trench, a thickness of the first material layers defines spaces between vertical structures of the plurality and further defines spaces between the sidewall of the trench and a vertical structure of the plurality that is adjacent to the sidewall.

**Claim 56 (New):** The imprinting apparatus of Claim 54, wherein each of the first material, the second material and a material of the semiconductor substrate are different from one another.

**Claim 57 (New):** The imprinting apparatus of Claim 54, wherein the alternating layers define an internal depth of the imprinting apparatus.

Appl. No. 10/826,056  
Resp./Amdt. dated Aug. 10, 2005  
Reply to Office Action of 05/16/05

Applicant has further amended line 8 to add 'of the plurality' after 'a vertical structure' to clarify this aspect of the claim for the Examiner.

The Examiner further queried, "It is not clear how a side of the vertical structure can face both of a side of an adjacent vertical structure and a trench sidewall?" Applicant appreciates the Examiner's thorough review of Claim 13 and has amended line 9 to remove 'or both' such that 'a side of the vertical structure' faces 'one of a side of an adjacent vertical structure and a trench sidewall'.

The Examiner further queried, "It is not clear where 'a trench sidewall' as cited on line 10 comes from and is located. Is there any relationship between this 'a trench sidewall' (line 10) to the 'the trench sidewalls' (lines 5-6)?" Applicant submits that 'a trench sidewall' on line 10 is a trench sidewall of 'the trench sidewalls' on line 5-6. This should be quite clear to the Examiner and does not require further clarification.

It is respectfully submitted that the Examiner's queries regarding Claim 13 do not rise to the level of a 35 U.S.C. 112, second paragraph, rejection, but instead should have been objections to Claim 13. Clearly the Examiner was able to discern the meets and bound of Claims 13-24, as originally filed. It should be noted that these amendments to Claim 13 in no way change the scope of Claim 13, as originally filed. In light of the above, the rejection of Claims 13-24 under 35 U.S.C. 112, second paragraph, should be withdrawn. Reconsideration and withdrawal of the 35 U.S.C. 112, second paragraph, rejection of Claims 13-24 are respectfully requested.

Claims 1-6, 8-17 and 19-24 were rejected under 35 U.S.C. 102(e) as being anticipated by, or in the alternative, under 35 U.S.C. 103(a) as obvious over Chou et al., U.S. Patent Application No. 2004/0156108 (hereinafter 'Chou et al.'). The Examiner contended that figures 13-17 and the corresponding text of Chou et al. disclose Applicant's claimed imprinting apparatus.

Applicant has cancelled Claims 10, 11, 22 and 23 herein, without prejudice. Therefore the rejection as to the cancelled claims is deemed moot. Moreover, Applicant has amended Claims 1, 8, 9, 13, 20 and 21 herein to better emphasize the features of embodiments of the invention illustrated in Applicant's Figure 3E. For



Appl. No. 10/826,056  
Resp./Amdt. dated Aug. 10, 2005  
Reply to Office Action of 05/16/05

example, base Claims 1 and 13 now recite that 'a material' of the vertical structures is 'different from a material of the semiconductor substrate'. Support for this amendment to Claims 1 and 13 can be found in Applicant's specification, page 15, lines 12-14 and lines 27-29, for example. In contrast, the vertical structures of Chou et al. in fig. 13a-c, which were pointed out by the Examiner, are made from, or are the same material as, the semiconductor substrate, since the vertical structures are formed by etching back the substrate. As such, Chou et al. fail to disclose or suggest the features of Applicant's Claims 1 and 13, as amended herein.

Claims 8 and 20 are amended to emphasize an embodiment of the imprinting apparatus that further comprises layers of an additional material ('a first material') alternating with one or more layers of the vertical structure material in the trench. The first material is different from the substrate material and the vertical structure material. Support for this amendment to Claims 8 and 20 can be found in Applicant's specification, page 15, lines 11-12, for example, and Figure 3E. It is respectfully submitted that Chou et al. fail to disclose or suggest an NIL apparatus that comprises an additional material that is different from the substrate material and the material of the vertical structures. Since Chou et al. fail to disclose the additional material layer, then Chou et al. fail to disclose or suggest that the additional material is disposed in the trench in layers that alternate with one or more layers of the material of the vertical structure. As such, Chou et al. fail to disclose or suggest that recited in Applicant's Claims 8 and 20, as amended herein.

Claims 9 and 21 are amended herein to recite examples of some materials used in the embodiments of the imprinting apparatus of Claims 8 and 20, respectively. Support for this amendment can be found in Claims 9 and 21, as originally filed. Since Chou et al. fail to disclose or suggest an NIL apparatus that comprises layers of an additional material, as described above for Claims 8 and 20, Chou et al. cannot and do not disclose or suggest examples of some materials used for the additional material layers that are recited in Applicant's Claims 9 and 21, as amended herein.

The Examiner contended, "(\* \*\* Notice that details about information of the first material does not carry patent weight the claimed structure [*sic*] since the first material is removed from the claimed structure)." However, amended Claims 8 and

Appl. No. 10/826,056  
Resp./Amdt. dated Aug. 10, 2005  
Reply to Office Action of 05/16/05

20 make clear that the claimed structure does include the first material, as illustrated in Figure 3E. The courts have held, "All words in a claim must be considered in judging the patentability of that claim against the prior art." *In re Wilson*, 424 F.2d 1382, 1385, 165 USPQ 494, 496 (CCPA 1970). Therefore, the Examiner's contention is moot in light of the amendments to Claims 8, 9, 20 and 21 and the 'first material' must be considered.

Rejected Claims 2-6 and 12 are dependent from and include all of the elements and/or limitations of base Claim 1. Rejected Claims 14-17, 19 and 24 are dependent from and include all of the elements and/or limitations of base Claim 13. The courts have held that if an independent base claim is non-obvious under 35 U.S.C. 103, any claim depending therefrom is likewise non-obvious. *In re Fine*, 837 F.2d 1071, 5 USPQ 2d 1596 (Fed. Cir. 1988). Since Chou et al. fail to disclose or suggest all of the elements of base Claim 1 and 13, then Chou et al. fail to disclose or suggest all of the elements of Claims 2-6, 12, 14-17, 19 and 24, which are respectively dependent therefrom.

The Federal Circuit has held, "[a]nticipation requires the disclosure in a single prior art reference of each element of the claim under consideration". *W.L. Gore & Associates v. Garlock*, 721 F.2d 1540, 220 USPQ 303 (Fed. Cir. 1983) *cert. denied*, 469 U.S. 851 (1984). Moreover, the courts have held, "[t]o establish *prima facie* obviousness of a claimed invention, all the claim limitations must be taught or suggested by the prior art." *In re Royka*, 490 F.2d 981, 180 USPQ 580 (CCPA 1974). See MPEP 2143.03 *All Claim Limitations Must Be Taught or Suggested*. Since Chou et al. fail to disclose or suggest all of the elements of Claims 1-6, 12-17, 19 and 24, then Chou et al. fail to anticipate or make obvious Claims 1-6, 12-17, 19 and 24.

In light of the above, reconsideration and withdrawal of the rejection of Claims 1-6, 8-17 and 19-24 under 35 U.S.C. 102(e) or in the alternative, under 35 U.S.C. 103(a) with respect to Chou et al. are respectfully requested.

New Claims 43-45 are dependent from Claim 8. New Claim 43 recites that the first material layers have a thickness that defines spaces between the vertical structures of the plurality and between each trench sidewall and an adjacent vertical structure of the plurality. Support for Claim 43 can be found in Applicant's

Appl. No. 10/826,056  
Resp./Amdt. dated Aug. 10, 2005  
Reply to Office Action of 05/16/05

specification, page 17, lines 17-28, for example, and Figure 3E. New Claim 44 recites that the layer of vertical structure material has vertically extending portions that are the vertical structures of the plurality. Support for Claim 44 can be found in at least Applicant's Figure 3E. New Claim 45 recites that the first material layers and the vertical structure material layer define an internal depth of the imprinting apparatus. Support for Claim 45 can be found in Applicant's specification, page 16, line 29 to page 17, line 4, and Figure 3E. New Claims 46-48 are ultimately dependent from Claim 13. New Claim 46 combines features of Claim 20 and new Claim 45. New Claim 47 incorporates the feature of new Claim 44 and is directly dependent from new Claim 46. New Claim 48 recites features of new Claim 43 and is directly dependent from new Claim 46. New Claim 49 is dependent from Claim 20 and recites a feature of new Claim 43. Support for new Claims 46-49 can be found in Applicant's specification, on the pages and in figures, cited *supra*, for new Claims 43-45. New Claims 50-53 and 54-57 are directed to a nano-imprinting apparatus that comprise some of the elements described above for Claims 1, 8, 13, 20 and new Claims 43-45. Support for new Claims 50-57 can be found in Applicant's specification, on the pages and in figures, cited *supra*, for amended Claims 1, 8, 13 and 20 and new Claims 43-45. It is respectfully submitted that Chou et al. fail to disclose or suggest the features of new Claims 43-57 for at least the same reasons provided above for amended Claims 1, 8, 13 and 20. Moreover, Applicant submits that the new claims do not add new matter and do not raise issues that were not already presented to the Examiner. Consideration and allowance of new Claims 43-57 are respectfully requested.

The Examiner rejected Claims 7 and 18 under 35 U.S.C. 103(a) as being unpatentable over Chou et al. in view of Schaper, U.S. Application No. 2003/0219992 (hereinafter 'Schaper'). The Examiner contended that although Chou et al. do not expressly disclose using a silicon-on-insulator wafer for the silicon layer, Schaper does show using the silicon-on-insulator wafer as the mold element for the imprinting apparatus. The Examiner concluded that it would be obvious to use the silicon layer with the (110) planar surface of Chou et al. as the silicon layer of the SOI of Schaper since it is a "convenient known substrate for mold element of the imprinting apparatus".

Appl. No. 10/826,056  
Resp./Amdt. dated Aug. 10, 2005  
Reply to Office Action of 05/16/05

Applicant respectfully traverses the rejection of Claims 7 and 18 under 35 U.S.C. 103(a) on the grounds that the Examiner failed to establish a *prima facie* case of obviousness with respect to Chou et al. in combination with Schaper. Specifically, the Examiner has failed to show, with respect to the rejected claims, one or more of 1) "some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings"; 2) "a reasonable expectation of success" in modifying or combining the teachings of the references; and 3) that the prior art references "teach or suggest all the claim limitations", as required by the courts. MPEP, Section 2142, *Establishing a Prima Facie Case of Obviousness*. Moreover, the Examiner failed to establish that the teaching or suggestion to make the claimed combination and the reasonable expectation of success are both "found in the prior art, and *not* based on applicant's disclosure" (*emphasis added*). *In re Vaeck*, 947 F.2d 488, 20 USPQ2d 1438 (Fed.Cir.1991).

It is respectfully submitted that the Examiner has at least failed to establish that Chou et al. in view of Schaper disclose or suggest *all* of the elements and/or limitations recited in Applicant's Claims 7 and 18, as required for establishing a *prima facie* case of obviousness. *In re Royka*, 490 F.2d 981, 180 USPQ 580 (CCPA 1974).

In particular, Claims 7 and 18 are dependent from and include all of the limitation of respective base Claims 1 and 13. As discussed above with respect to the 35 U.S.C. 102(e)/103(a) rejection, Chou et al. fail to disclose *all* of the elements and/or limitations recited in base Claims 1 and 13, as amended herein. Schaper fail to add to that lacking in the teachings of Chou et al., such that all claimed elements and/or limitations of base Claims 1 and 13 would be disclosed by the combined teachings of Chou et al. and Schaper. As such, Chou et al. in combination with Schaper also fail to disclose *all* of the elements and/or limitations recited in dependent Claims 7 and 18, as required by the Federal Circuit for establishing *prima facie* obviousness. *In re Royka*, cited *supra*; and *In re Fine*, cited *supra*.

In particular, for the reasons set forth above, Chou et al. fail to disclose that the material of the vertical structures is different from the material of the substrate, as

Appl. No. 10/826,056  
Resp./Arndt. dated Aug. 10, 2005  
Reply to Office Action of 05/16/05

claimed by Applicant. Moreover, Schaper, like Chou et al., also does not disclose that the material of the vertical structures is different from the material of the substrate. As such, and without more, Chou et al. in combination with Schaper cannot disclose that recited in Applicant's base Claims 1 and 13. Likewise, contrary to that contended by the Examiner, Chou et al. in combination with Schaper respectfully cannot and do not disclose *all* of the elements and/or limitations recited in Claims 7 and 18 if the elements of respective Claims 1 and 13 are not disclosed by the combined teachings.

A failure to disclose all elements of the rejected claim is, in and of itself, sufficient grounds to defeat *prima facie* obviousness. For at least the reasons set forth above, Chou et al. in view of Schaper fail to render Claims 7 and 18 obvious and the rejection should be withdrawn.

Moreover, as to a motivation to modify or combine the references, MPEP §2143.01 *Suggestion or Motivation to Modify the References* states, "Obviousness can only be established by combining or modifying the teachings of the prior art to produce the claimed invention where there is some teaching, suggestion, or motivation to do so found either explicitly or implicitly in the references themselves or in the knowledge generally available to one of ordinary skill in the art. 'The test for an implicit showing is what the combined teachings, knowledge of one of ordinary skill in the art, and the nature of the problem to be solved as a whole would have suggested to those of ordinary skill in the art.' *In re Kotzab*, 217 F.3d 1365, 1370, 55 USPQ2d 1313, 1317 (Fed. Cir. 2000). See also *In re Fine*, 837 F.2d 1071, 5 USPQ2d 1596 (Fed. Cir. 1988); *In re Jones*, 958 F.2d 347, 21 USPQ2d 1941 (Fed. Cir. 1992)". "The mere fact that references can be combined or modified does not render the resultant combination obvious unless the prior art also suggests the desirability of the combination. *In re Mills*, 916 F.2d 680, 16 USPQ2d 1430 (Fed. Cir. 1990)". MPEP §2143.01, cited *supra*.

It is respectfully submitted that the Examiner has further failed to show that the prior art also suggests the desirability of the combination in rejecting Claims 7 and 18 under Chou et al. in view of Schaper. *In re Mills*, cited *supra*. In particular, Examiner's contended motivation of "convenient known substrate for mold element of the imprinting apparatus" does not qualify as a motivation according to the Federal

Appl. No. 10/826,056  
Resp./Amdt. dated Aug. 10, 2005  
Reply to Office Action of 05/16/05

Circuit. *In re Kotzab*; *In re Fine*; and *In re Jones*, each cited *supra*. Hence, Applicant respectfully submits that the Examiner has further failed to provide a proper suggestion or motivation to modify or combine the reference teachings that is found either in the references themselves or in the knowledge generally available to one of ordinary skill in the art. Notwithstanding that Chou et al. in view of Schaper fail to disclose all elements of Claims 7 and 18, a lack of a motivation to combine the references also is, in and of itself, sufficient grounds to defeat *prima facie* obviousness and therefore, the rejection should be withdrawn.

Thus, Applicant respectfully submits that the Examiner has failed to establish *prima facie* obviousness of Applicant's Claims 7 and 18 with respect to Chou et al. in view of Schaper for at least the reasons given hereinabove. Reconsideration and withdrawal of the unsupported rejection of Claims 7 and 18 are respectfully requested.

In summary, Claims 1-42 were pending in the application. Previously withdrawn Claims 25-42 and Claims 10, 11, 22 and 23 are cancelled herein, without prejudice. New Claims 43-57 are added. Claims 1, 8, 9, 13, 20 and 21 are amended. Applicant respectfully submits that Claims 1-9, 12-21, 24 and 43-57 are in condition for allowance. It is respectfully requested that Claims 1-9, 12-21, 24 and 43-57 be allowed, and that the application be passed to issue at an early date.

Should the examiner have any questions regarding the above, please contact the undersigned, Elizabeth E. Leitereg, telephone number (775) 849-3085.

Respectfully submitted,  
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#### CERTIFICATE OF TRANSMISSION

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